

Appl. No.: 09/924,973  
Amdt. Dated: August 7, 2005  
Off. Act. Dated: February 7, 2005

## **AMENDMENTS TO THE SPECIFICATION:**

Please insert the following paragraph in the specification at page 17, line 10  
(*following the description of FIG. 9*) with the following paragraph:

“FIG. 10A-10B are flow diagrams of device programming and operation according to an embodiment of the present invention.”

Please replace the paragraph at page 17, line 11 with the following amended paragraph:

“Referring more specifically to the drawings, for illustrative purposes the present invention is embodied in the apparatus generally shown in FIG. 2 through FIG. [[9]] 10B. It will be appreciated that the apparatus may vary as to configuration and as to details of the parts without departing from the basic concepts as disclosed herein.”

Please insert the following paragraphs at page 30, line 13 for describing added FIG. 10A and FIG. 10B:

“FIG. 10A illustrates by way of example embodiment the programming of an array of optical elements configured according to the present invention. Block 170 refers to connecting the optical element into an array prior to commencing in-situ programming in the target array. The address to which the optical elements according to the present invention are responsive is programmed onto the optical devices when they are in their target configuration. In the array configuration the optical element

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receives signals which drive its addressing. These same signals are received by each of the optical device elements contained in the array.

In block 172 the optical devices enter programming mode, wherein they maintain an address count at block 174. When the circuit detects receiving a programming signal at block 176, depicted as being received from an optical detector in one embodiment, it commences to load an array address (first address) into a memory, such as non-volatile memory. This first address is loaded with the current count value maintained in response to counting received clocks, as well as in response to clock control signals such as reset. This completes the general aspect of programming the array address into the display element. As a consequence of the in-situ array position addressing process, the optical device becomes configured to generate optical outputs based on data received in association an address (a second address) which matches the programmed into memory.

FIG. 10B illustrates by way of example embodiment the process of outputting data from the optical element in response to data and clocking being received by the device.

Represented in block 180, counters on the device are driven to maintain an address. This address, now referred to as a second address, is compared with the address stored in memory as a first address, as per block 182. If no match exists the circuit just continues counting, represented by a return to block 180. Upon matching the second address to the first address, bits of data are read in from the data signal

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being received by each element in the array as per block 184. The data bits are then latched for output by the optical element at block 186. At some point, such as upon receiving a counter reset clock, the data is output to drive the optical elements and the counter is reset.

The device continues to repeat the process of counting up clocks and attempting to find a match between first and second addresses wherein it knows the data on the input signal is intended for output at its array position address."